PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG/14/8475
Dated 16 May 2014

Assembly and Testing transfer from the ST plant of

Longgang to ST Shenzhen

Table 1. Change Implementation Schedule

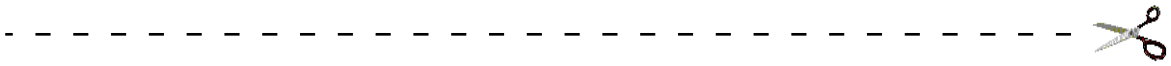
Forecasted implementation date for change	13-Aug-2014
Forecasted availability date of samples for customer	09-May-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	09-May-2014
Estimated date of changed product first shipment	20-Aug-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly location change, Package assembly process change, Testing location change
Reason for change	To improve service to ST Customers and standardize manufacturing processes
Description of the change	Continuing in the already announced plan of consolidating the assembly and testing activities for the products housed in TO-247 and DO-247 packages, ST is glad to announce the transfer of the production lines from the ST plant of Longgang to the ST plant of Shenzhen. The change will also benefit of the standardization for those packages of the electroplating process already massively used for all the other power packages.
Change Product Identification	"GK" marked on the package
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG/14/8475**
Please sign and return to STMicroelectronics Sales Office	**Dated 16 May 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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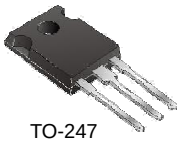
DOCUMENT APPROVAL

Name	Function
Giuffrida, Antonino	Marketing Manager
Martelli, Nunzio	Product Manager
Vitali, Gian Luigi	Q.A. Manager

IPG Group

Assembly and Testing transfer from the ST plant of Longgang to ST Shenzhen and introduction of the leads electroplating finishing for the products housed in TO-247 and DO-247 packages.

Packages typology



TO-247

DO-247

WHAT:

Continuing in the already announced plan of consolidating the assembly and testing activities for the products housed in TO-247 and DO-247 packages, ST is glad to announce the transfer of the production lines from the ST plant of Longgang to the ST plant of Shenzhen.
The change will also benefit of the standardization for those packages of the electroplating process already massively used for all the other power packages.

For the complete list of the part numbers affected by these changes, please refer to the attached Products List.

Samples, of the test vehicle from the ST plant of Shenzhen are available right now upon request for immediate customer qualification, while the full availability of products will be granted from wk 20 2014 onwards. Any other sample request will be granted upon request

WHY:

To improve service to ST Customers and standardize manufacturing processes for the power packages typology.

HOW:

By transferring the existing equipments from the Longgang ST plant to the Shenzhen one.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant product's datasheets.
There are as well neither modifications in the packing modes nor in the standard delivery quantities.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

WHEN:

Production start and first shipments will occur as per the scheduling indicated in the tables below.

Affected Product Types	Samples	1st Shipment
Power MOSFET	**Now**	**Wk 32**
Power Bipolar	**Now**	**Wk 32**
IGBT	**Now**	**Wk 32**
Rectifier	**Now**	**Wk 32**

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts produced in ST Shenzhen will be ensured by the Q.A. number and plant code identification “GK” marked on the package, as illustrated in the below picture:

Package marking example

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change.
After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer’s written agreement.

Reliability Report

Qualification of assembly and Testing transfer from Longgang ST plant to Shenzhen ST plant for rectifier products in TO247&DO247 package.

General Information	
Product Description	*Rectifier*
Product Group	*IPG*
Product division	*ASD&IPAD*
Package	*TO-247* *DO-247*
Maturity level step	*Qualified*

Locations	
Wafer fab	*ST TOURS (FRANCE)* *ST AMK (SINGAPORE)*
Assembly plant	*ST SHENZHEN (CHINA)*
Reliability Lab	*ST Tours*
Reliability assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	28/04/2014	8	Aude DROMEL	Jean-Paul REBRASSE	

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

DUT	Device Under Test
PTV	Product Test Vehicle
PCB	Printed Circuit Board
SS	Sample Size
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB	Temperature Humidity Bias
IOLT	Intermittent Operating Life Test
PCT/AC	Pressure Cooker Test (Autoclave)
RSH	Resistance to Solder Heat
SD	Solderability

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify the assembly and testing transfer from the ST plant of Longgang to ST plant of Shenzhen for the rectifiers products in TO-247 and DO-247 packages.

The reliability test methodology used follows the JESD47-H: « Stress Test Driven Qualification Methodology ». Rectifier diodes perimeter is covered through 5 different test vehicles including turbo/bipolar diodes and Schottky barrier diodes. These test vehicles have been chosen to include the most critical parameters for reliability (die size, highest voltage, etc.)
The following reliability tests are:

- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- TC and IOLT to ensure the mechanical robustness of the products.
- THB/AC to check the robustness to corrosion and the good package hermeticity.
- RSH and Solderability

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

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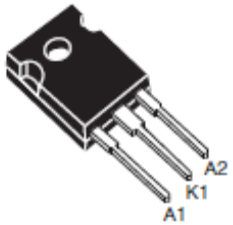
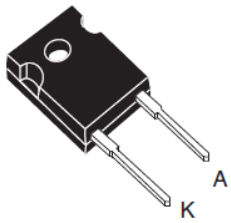
4 DEVICES CHARACTERISTICS

4.1 Devices descriptions

All rectifiers (bipolar, turboswitch, power shottky in silicon and silicon carbide) assembled in TO-247 and DO-247 packages.



TO-247



DO-247

4.2 Construction Note

	STTHxxxxW
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS FRANCE
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS FRANCE
Assembly information	
Assembly site	ST SHENZHEN -CHINA
Package description	TO-247 & DO-247
Molding compound	ECOPACK®2 (“Halogen-free”)
Lead finishing material	Tin 100%
Final testing information	
Testing location	ST SHENZHEN CHINA

	STPSxxxxW
Wafer/Die fab. information	
Wafer fab manufacturing location	ST AMK SINGAPORE or ST TOURS FRANCE
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST AMK SINGAPORE or ST TOURS FRANCE
Assembly information	
Assembly site	ST SHENZHEN -CHINA
Package description	TO-247
Molding compound	ECOPACK®2 (“Halogen-free”)
Lead finishing material	Tin 100%
Final testing information	
Testing location	ST SHENZHEN -CHINA

	STPSCxxxW
Wafer/Die fab. information	
Wafer fab manufacturing location	ST CATANIA ITALY
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST CATANIA ITALY
Assembly information	
Assembly site	ST SHENZHEN -CHINA
Package description	TO-247
Molding compound	ECOPACK®2 ("Halogen-free")
Lead finishing material	Tin 100%
Final testing information	
Testing location	ST SHENZHEN -CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Part Number	Package	Technology family	Comments
1	STTH100W06CW	TO-247	Rectifier Turboswitch	-Big die -Ribbon bonding
2	STPSC2006CW	TO-247	Power Shottky SiC	-Big die SiC -Dual configuration
3	STTH3012W	DO-247	Rectifier Turboswitch	-Highest voltage -2-leads package
4	PS80170CW	TO-247	Power Schottky	-Highest voltage Schottky -Big die -Multi-wires bonding
5	YPS4045CW	TO-247	Power Schottky	-Low voltage Schottky -Standard Al 20mils bonding

Detailed results in below chapter will refer to these references.

5.2 Test plan and results summary

Test	Std ref.	Conditions	SS	Steps / duration	Failure/SS				
					L1	L2	L3	L4	L5
HTRB	JESD22 A-108	VR = 0.8xVRRM = 960V Tj = 175°C for GD1 150°C for other lots	231	1000h		0/77	0/77	0/77	
THB	JESD22 A-101	85% RH, 85°C VR=100V	231	1000h	0/77	0/77			0/77
TC	JESD22 A-104	-65 / +150°C 2 cycles/hour	231	1000cy	0/77	0/77		0/77	
AC	JESD22 A-102	121°C 2bar 100% RH	231	96h	0/77	0/77		0/77	
IOLT	Mil Std 750 method 1037	ΔTc = 85°C t_{on} = t_{off} = 300s	231	6kcy	0/77	0/77			0/77
RSH	JESD22 B-106	Oil bath* 245°C 10sec/dip 2 dips	10	N/A	0/10				
SD	ST internal 0018688	Wet ageing + Sn/Pb bath Wet ageing + Sn/Ag/Cu bath	30		0/15 0/15				

*oil bath dipping with all the package dipped is assumed to be more stressing than lead dipping in solder bath in terms if die temperature profile.

6 ANNEXES

6.1 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
PCT Pressure Cooker Test (Autoclave)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
RSH Resistance to Solder Heat	Package is dipped by the leads 2 times in a solder bath.	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
SD Solderability	Wet ageing + dipping in a solder bath. Assessment by visual inspection of the leads.	To check package ability to be soldered with no difficulty. To simulate

Reliability Report

Assembly and Testing transfer from the ST plant of Longgang to ST Shenzhen and introduction of the leads electroplating finishing for the products housed in TO-247 package.

General Information	
Product Lines:	M5F9 – M264 – 2F6B – 2F69 – IV68+E61L – BA21
Product Families:	Power MOSFET (M5F9 – M264 – 2F6B – 2F69) IGBT (IV68(IGBT) + E61I(diode)) Power BIPOLAR (BA21)
P/Ns:	STW78N65M5 (M5F9) STW19NM60N (M264) STW47NM60ND (2F6B) STW55NM60ND (2F69) STGW39NC60VD (IV68) TIP35C (BA21)
Product Group:	IPG
Product division:	Power Transistor Division
Package:	TO-247
Silicon Process techn.:	MDmesh™ V Power MOSFET MDmesh™ II Power MOSFET FDmesh™ II Power MOSFET IGBT Power BIPOLAR

Locations	
Wafer Diffusion Plants:	*Ang Mo Kio (Singapore)* *Catania CT6/CT8 (Italy)*
EWS Plants:	*Ang Mo Kio (Singapore)* *Catania (Italy)*
Assembly and testing plant:	*ST Shenzhen (China)*
Reliability Lab:	*IPG-PTD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	May2014	16	A. Settinieri	C. Cappello	First issue

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability evaluation for assembly and testing transfer from the ST plant of Longgang to ST Shenzhen and introduction of the leads electroplating finishing for the products housed in TO-247 package.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET
IGBT
N-channel Power BIPOLAR

4.2 Construction note

D.U.T.: STW78N65M5 LINE: M5F9 PACKAGE: TO-247

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania CT8 (Italy)
Technology	MDmesh™ V Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	1041 x 6810 μm^2
Metal	AlCu/Ti/TiN
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania CT8 (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Source Ribbon Al
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	STS Shenzhen (China)
Tester	TESEC

D.U.T.: STW19NM60N LINE: M264 PACKAGE: TO-247

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	MDmesh™ II Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	4400 x 3200 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	STS Shenzhen (China)
Tester	TESEC

D.U.T.: STW47NM60ND LINE: 2F6B PACKAGE: TO-247

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania CT6 (Italy)
Technology	FDmesh™ II Power MOSFET
Die finishing back side	Ti/Ni/Au
Die size	8800 x 5760 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania CT6 (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Source Ribbon Al
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	STS Shenzhen (China)
Tester	TESEC

D.U.T.: STW55NM60ND LINE: 2F69 PACKAGE: TO-247

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania CT6 (Italy)
Technology	FDmesh™ II Power MOSFET
Die finishing back side	Ti/Ni/Au
Die size	1039 x 6850 µm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania CT6 (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Source Ribbon Al
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	STS Shenzhen (China)
Tester	TESEC

D.U.T.: STGW39NC60VD LINE: IV68 PACKAGE: TO-247

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	Igbt Fast
Die finishing back side	Cr/Ni/Ag
Die size	5300 x 6580 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	STS Shenzhen (China)
Tester	TESEC

D.U.T.: TIP35C LINE: BA21 PACKAGE: TO-247

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	Power BIPOLAR NPN
Die finishing back side	Ti/Ni/Ag
Die size	4030 x 3680 μm^2
Metal	Al/Si
Passivation type	PSG

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	STS Shenzhen (China)
Tester	TESEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STW78N65M5	M5F9	Power MOSFET
2	STW19NM60N	M264	
3	STW47NM60ND	2F6B	
4	STW55NM60ND	2F69	
5	STGW39NC60VD	IV68+E61I	IGBT
6	TIP35C	BA21	Power BIPOLAR

5.2 Reliability test plan summary

Lot. 1 - D.U.T.: STW78N65M5 LINE: M5F9 PACKAGE: TO-247

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 1
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=520V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 25V	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	77	168 H 500 H 1000 H	0/77
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy	0/77
TF/IOL	N	Mil-STD 750D Method 1037	ΔTC=105°C Ton / Toff = 5min	77	6K cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

Lot. 2 - D.U.T.: STW19NM60N LINE: M264 PACKAGE: TO-247

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 2
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=480V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 25V	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	77	168 H 500 H 1000 H	0/77
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy	0/77
TF/IOL	N	Mil-STD 750D Method 1037	ΔTC=105°C Ton / Toff = 5min	77	6K cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

Lot. 3 - D.U.T.: STW47NM60ND LINE: 2F6B PACKAGE: TO-247

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 3
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=175°C Vdss=480V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 20V	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	77	168 H 500 H 1000 H	0/77
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy	0/77
TF/IOL	N	Mil-STD 750D Method 1037	ΔTC=105°C Ton / Toff = 5min	77	6K cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

Lot. 4 - D.U.T.: STW55NM60ND LINE: 2F69 PACKAGE: TO-247

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 4
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=480V	77	168 H	0/77
					500 H	
					1000 H	
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 25V	77	168 H	0/77
					500 H	
					1000 H	
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	77	168 H	0/77
					500 H	
					1000 H	
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy	0/77
					200 cy	
					500 cy	
TF/IOL	N	Mil-STD 750D Method 1037	ΔTC=105°C Ton / Toff = 5min	77	6K cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

Lot. 5 - D.U.T.: STGW39NC60V LINE: IV68 (IGBT) PACKAGE: TO-247
E61I (diode)

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 5
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=480V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 20V	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	77	168 H 500 H 1000 H	0/77
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy	0/77
TF/IOL	N	Mil-STD 750D Method 1037	ΔTC=105°C Ton / Toff = 5min	77	6K cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

Lot. 6 - D.U.T.: TIP35C LINE: BA21 PACKAGE: TO-247

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 5
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=80V	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
H3TRB	N	JESD22 A-101	Ta=85°C Rh=85%, Vdss=80V	77	168 H 500 H 1000 H	0/77
TC	N	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy	0/77
TF/IOL	N	Mil-STD 750D Method 1037	ΔTC=105°C Ton / Toff = 5min	77	6K cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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